Listing of Claims:

This listing of claims lists the claims currently pending in the present application.

1-32. (Cancelled)

33. (Previously presented) A memory cell, comprising:

a column of epitaxial layers having a first dimension along a first axis and a second dimension along a second axis perpendicular to the first axis;

an oxide formed under the columns of epitaxial layers;

a storage device formed in a lower layer of the epitaxial layers of the columns; and

an access element formed on a surface of the column, the access element having a dimension in the first direction less than the first dimension of the column.

34. (Previously presented) The memory cell of claim 33 wherein the storage device comprises a bipolar junction transistor.

35. (Previously presented) The memory cell of claim 33 wherein the access element comprises a vertical p-channel MOS transistor.

36. (Previously presented) The memory cell of claim 33 wherein the first dimension of the column corresponds to a feature size of the memory cell.

37. (Previously presented) The memory cell of claim 33 wherein the dimension of the vertical access element in the first direction is less than half the first dimension of the column.

38. (Previously presented) The memory cell of claim 33 wherein the storage device comprises a bipolar junction transistor and the access element comprises a vertical p-

channel MOS transistor having a source formed in the same epitaxial layer in which the bipolar junction transistor is formed.

39. (Previously presented) A memory cell, comprising:

a column of epitaxial layers perpendicular to a substrate surface, the column having a lower epitaxial layer on which the other epitaxial layers are formed, the column further having a first dimension in a first direction and a second dimension in a second direction perpendicular to the first direction;

a storage device formed in the lower epitaxial layer of the column; and

a vertical access element formed on a surface of the column, the vertical access element having a dimension in the first direction less than the first dimension of the column.

40. (Previously presented) The memory cell of claim 39 wherein the storage device comprises a bipolar junction transistor.

41. (Previously presented) The memory cell of claim 39 wherein the vertical access element comprises a vertical p-channel MOS transistor.

42. (Previously presented) The memory cell of claim 39 wherein the first dimension of the column corresponds to a feature size of the memory cell.

43. (Previously presented) The memory cell of claim 39 wherein the dimension of the vertical access element in the first direction is less than half the first dimension of the column.

44. (Previously presented) The memory cell of claim 39 wherein the storage device comprises a bipolar junction transistor and the vertical access element comprises a vertical p-channel MOS transistor having a source formed in the same epitaxial layer in which the bipolar junction transistor is formed.

45. (Previously presented) An array of memory cells, comprising:

a plurality of columns of epitaxial layers formed on a substrate surface, the columns of epitaxial layers having a first dimension along a first axis and second dimension along a second axis perpendicular to the first axis;

a plurality of trenches separating the plurality of columns, each trench having a width in the direction of the first axis;

a plurality of storage devices, each storage device formed in a lower layer of the epitaxial layers of the columns; and

a plurality of access elements, each access element formed within a trench and on a surface of a respective column and having a dimension in the direction of the first axis that is less than the first dimension of the columns.

46. (Previously presented) The array of memory cells of claim 45 wherein a first access element for a first memory cell and a second access element for a second memory cell are formed in the same trench.

47. (Previously presented) The array of memory cells of claim 45 wherein each of the storage devices comprises a bipolar junction transistor.

48. (Previously presented) The array of memory cells of claim 45 wherein each of the vertical access elements comprises a vertical p-channel MOS transistor.

49. (Previously presented) The array of memory cells of claim 45 wherein the first dimension of each column corresponds to a feature size of the memory cells.

50. (Previously presented) The array of memory cells of claim 45 wherein each of the storage devices comprises a bipolar junction transistor and each of the vertical access elements comprises a vertical p-channel MOS transistor having a source formed in the same epitaxial layer in which the bipolar junction transistor is formed.